FIG. 1

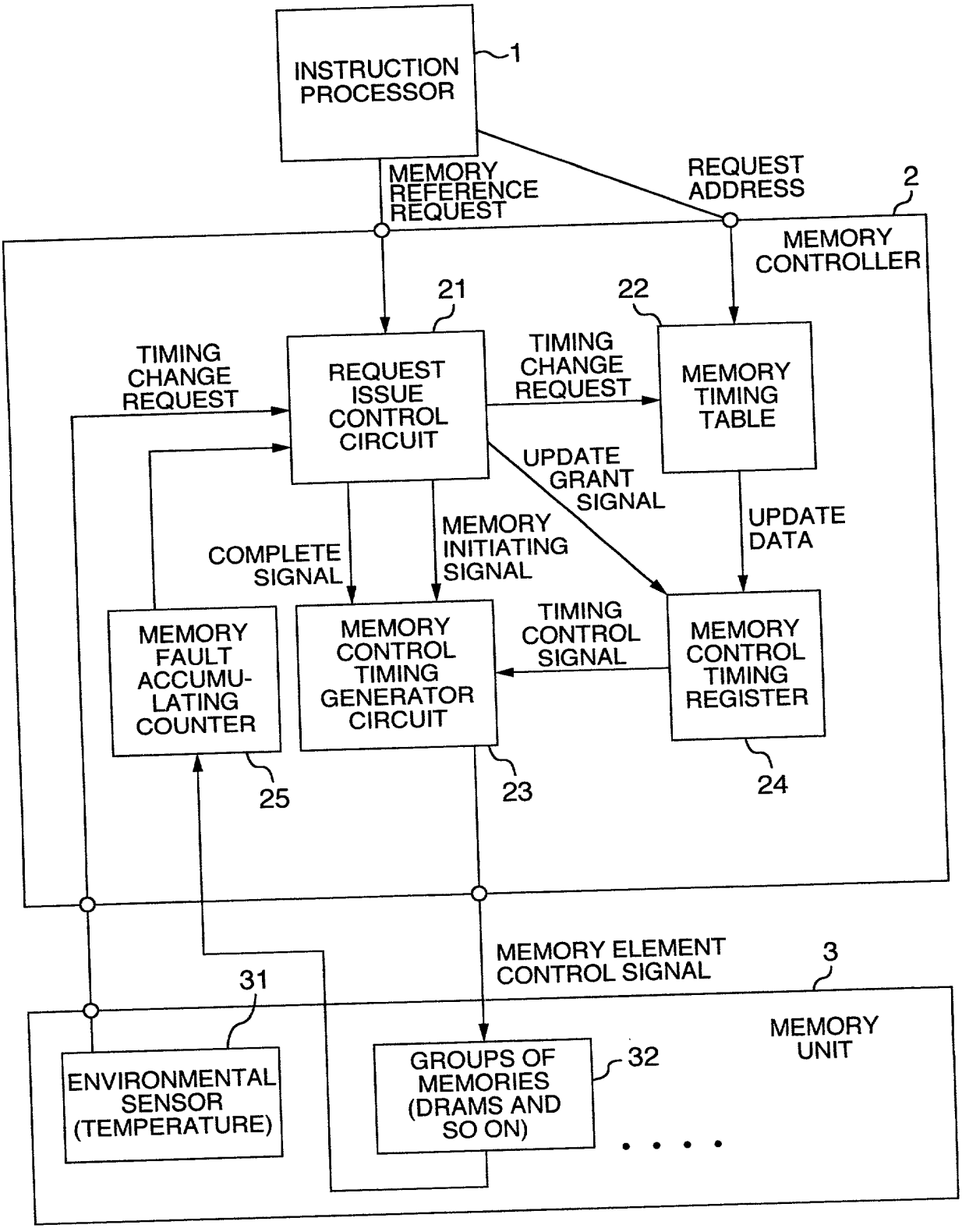

INSTRUCTION PROCESSOR
1
MEMORY REFERENCE REQUEST
REQUEST ADDRESS
2
MEMORY CONTROLLER
21
22
TIMING CHANGE REQUEST
REQUEST ISSUE CONTROL CIRCUIT
TIMING CHANGE REQUEST
MEMORY TIMING TABLE
UPDATE GRANT SIGNAL
UPDATE DATA
COMPLETE SIGNAL
MEMORY INITIATING SIGNAL
MEMORY FAULT ACCUMU-LATING COUNTER
MEMORY CONTROL TIMING GENERATOR CIRCUIT
TIMING CONTROL SIGNAL
MEMORY CONTROL TIMING REGISTER
25
23
24
MEMORY ELEMENT CONTROL SIGNAL
3
31
MEMORY UNIT
ENVIRONMENTAL SENSOR (TEMPERATURE)
GROUPS OF MEMORIES (DRAMS AND SO ON)
32
. . . .

FIG. 2

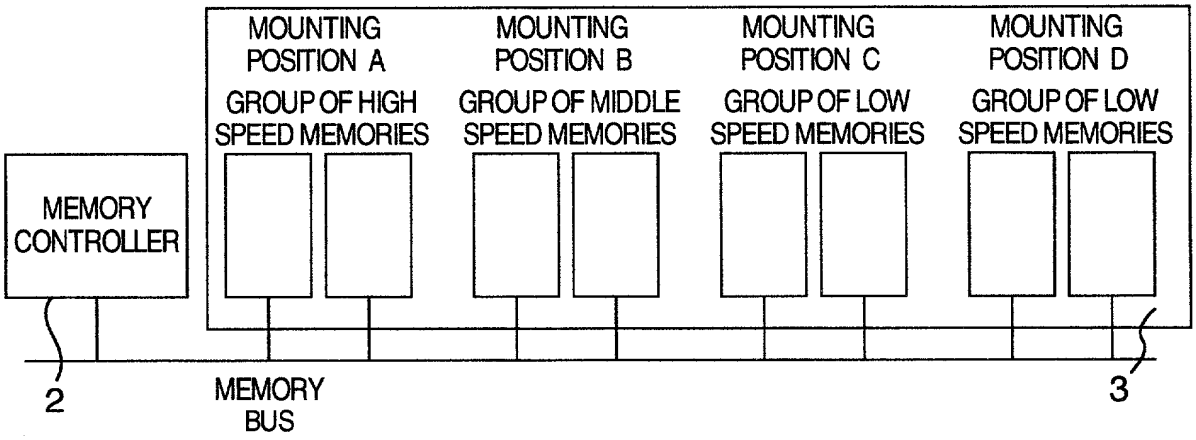


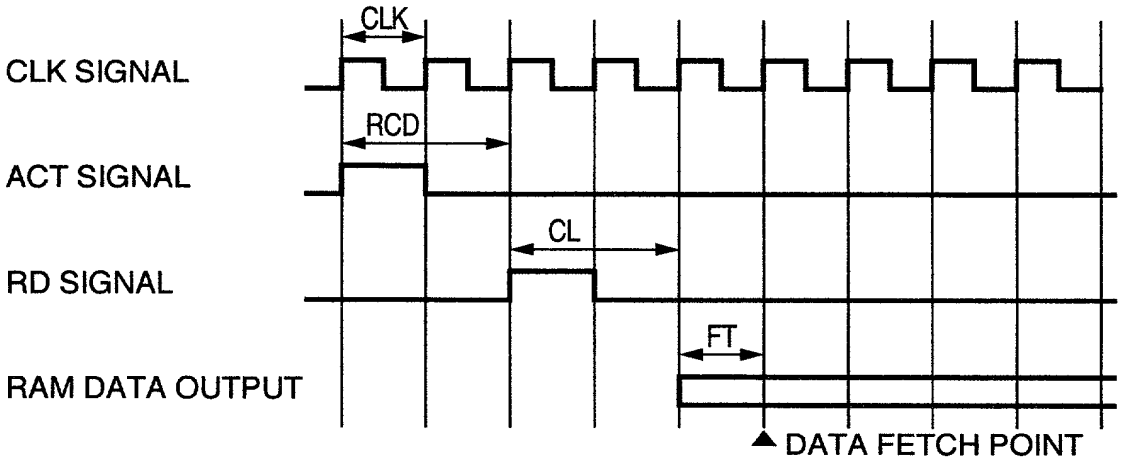
FIG. 3

MOUNTING POSITION	MEMORY TIMING PARAMETERS			
	CLK	RCD	CL	FT
A	10ns	20ns	20ns	10ns
B	10ns	20ns	30ns	10ns
C	15ns	30ns	30ns	10ns
D	15ns	30ns	45ns	15ns

22

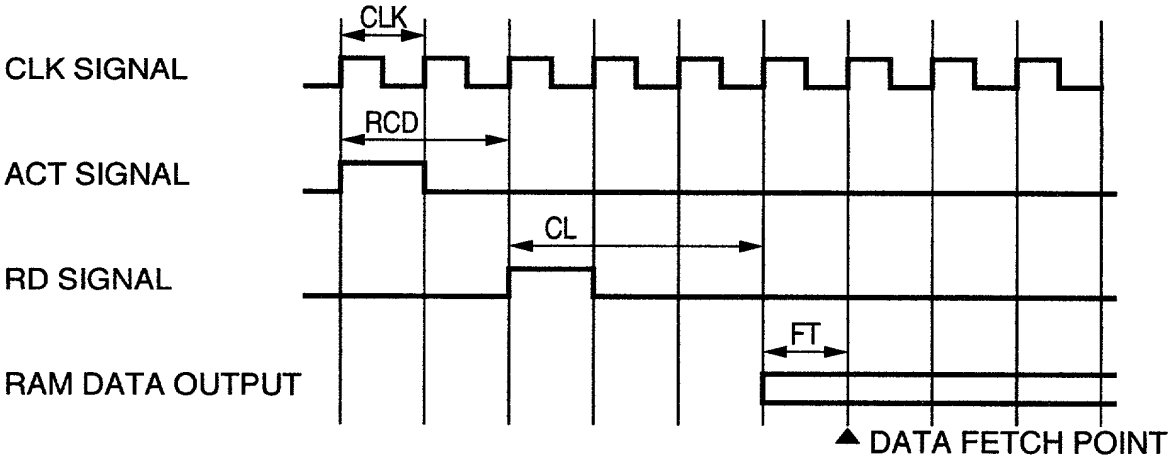
CONTENTS OF MEMORY TIMING TABLE

FIG. 4A



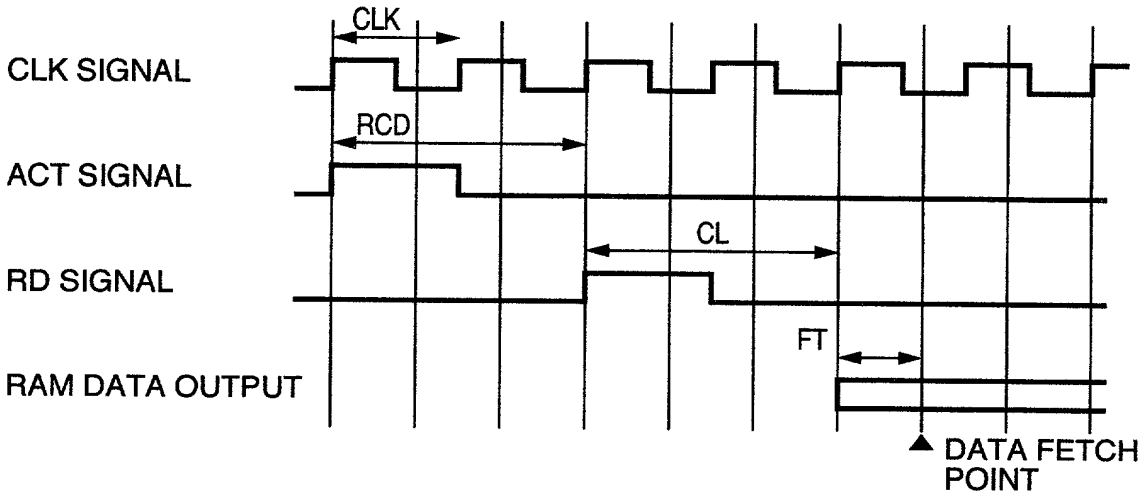
SDRAM OPERATION TIMING AT MOUNTING POSITION A

FIG. 4B



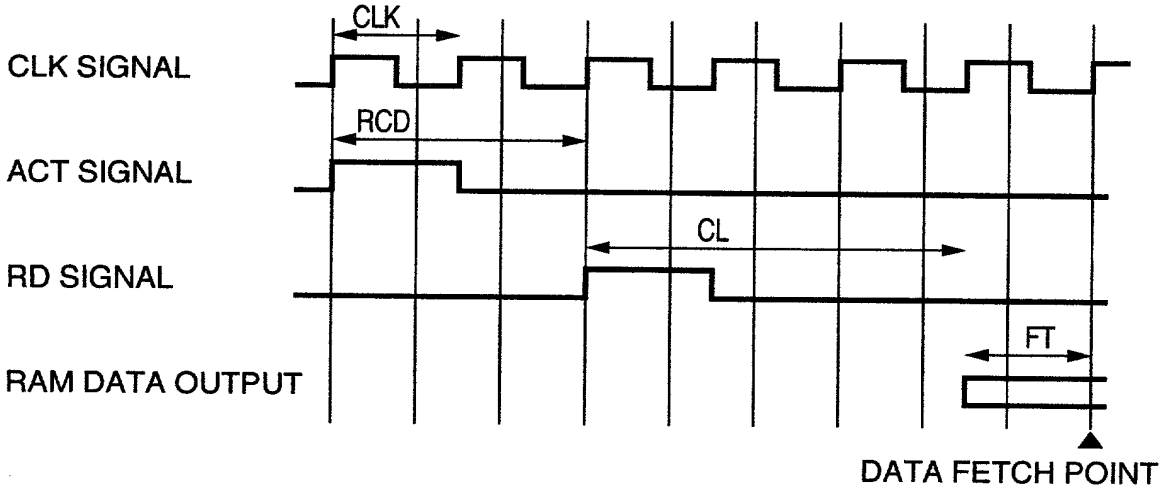
SDRAM OPERATION TIMING AT MOUNTING POSITION B

FIG. 5A



SDRAM OPERATION TIMING AT MOUNTING POSITION C

FIG. 5B



SDRAM OPERATION TIMING AT MOUNTING POSITION D